UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,883	08/27/2003	Satoru Yamada	16995	4882

23389 7590 04/21/2005

SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
SUITE 300
GARDEN CITY, NY 11530

EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,883	YAMADA ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8 and 10* is/are rejected.

7)☒ Claim(s) *6,7,9 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. This objection was made in the previous Office action but it has not been addressed by the applicant.

Claim Objections

4. Claims 9 and 11 are objected to because of the following informalities: the phrases "having the lowest Fermi level is disposed" (in claims 9 and 11) and "having the highest Fermi level is disposed" (in claim 11) appear to be grammatically incorrect. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5, 8, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schwalke (USPN 5,932,919) in view of Takashima et al. (USPN 5,953,246) and further in view of Shau (USPN 6,216,246 B1) and further in view of Noble et al. (USPN 6,573,169 B2).

7. In reference to claims 1-4 and 8, Schwalke (USPN 5,932,919) discloses a similar device and its process of fabrication. Figure 1H of Schwalke discloses a low threshold voltage CMOS transistor pair for use in a DRAM device. The transistor on the left is an n-channel transistor with an n-type gate (26). The transistor on the right is a p-channel transistor with a gate (30) with both n-type and p-type doping. This gate (30) is mostly n-type (column 3, lines 1-6) with a higher than average concentration achieved by ion implantation (column 2, lines 54-56). Since p-type materials have Fermi levels near the valence band and n-type materials have Fermi levels near the conduction band, it is understood that the gate (30) for the p-channel transistor has a Fermi level lower than that of the gate (26) for the n-channel transistor by virtue of the combination of the n-type and p-type impurities within its gate (30) when compared to the strictly n-type gate (26) of the n-channel transistor. Schwalke does not disclose a third transistor with a p-type polysilicon gate having a low Fermi level. However the use of such transistors in a DRAM is well known in the art. Takashima et al. (USPN 5,953,246, hereinafter referred to as the "Takashima" reference) discloses an n-channel transistor with a p-type gate. Takashima discloses that such a gate allows the transistor to have a high threshold voltage (column 14, lines 17-21). Furthermore, Shau (USPN 6,216,246 B1) discloses

that it is well known in the art that memory transistors have a higher threshold voltage than that of the peripheral circuitry for the benefits of higher voltage tolerance, leakage current reduction, and high performance peripheral logic circuitry (column 1, lines 41-47). In view of Shau and Takashima, it would therefore be obvious to use an n-channel transistor with a p-type gate. Takashima does not disclose the use of a polysilicon gate material for the p-type gate but the use of polysilicon as a gate material is well known in the art. Noble et al. (USPN 6,573,169 B2, hereinafter referred to as the "Noble" reference) discloses that the use of a polysilicon gate in a transistor leads to a more reliable device with superior drains and sources (column 1, lines 50-54). In view of Noble, it would therefore be obvious to use polysilicon as the gate material in order to attain the benefit of a more reliable transistor.

8. With regard to claim 5, Schwalke discloses a method of fabrication which meets these limitations regarding the masks (column 2, lines 52-67 and column 3, 25-33).

9. In reference to claim 10, the limitation "wherein the concentration of the p type impurity that is injected into the first N surface channel is reduced such that a pn junction leak current is reduced" has no patentable weight since a structural limitation has not been described. Therefore claim 10 is not patentable over the Schwalke, Takashima, Shau, and Noble references.

Allowable Subject Matter

10. Claims 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a method of fabricating a semiconductor device having a first p-type polysilicon gate at a first Fermi level, a first n-type polysilicon gate at a higher Fermi level than the first p-type polysilicon gate, and a second n-type polysilicon gate with both n-type and p-type doping which has a Fermi level that is between the first p-type polysilicon gate and the first n-type polysilicon gate where the dopants (both n-type and p-type) of the second n-type polysilicon gate are simultaneously activated.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800